IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor integrated circuit device comprising:

a data line group including a plurality of data lines;

a first bit line group including a plurality of bit lines;

a first column gate circuit that electrically connects the first bit line group to the data line group according to a first column selection signal;

a second bit line group including a plurality of bit lines:

a second column gate circuit that electrically connects the second bit line group to the data line group according to a second column selection signal different from the first column selection signal;

a plurality of word lines intersecting the plurality of bit lines included in the first and second bit line groups; and

a plurality of memory cells including magneto-resistive elements and adapted to be electrically connected to a plurality of bit lines included in the first and second bit line groups and selected by the plurality of word lines, spinning directions of the magneto-resistive elements being perpendicular to the plurality of bit lines included in the first and second bit line groups as seen on a plan view[[.]] ,wherein data is written to the plurality of memory cells by making a write electric current flow to the plurality of bit lines of the first or second bit line group, writing data being determined by a direction of the write electric current flowing to the plurality of bit lines of the first or second bit line group.

Claim 2 (Withdrawn): A semiconductor integrated circuit device comprising:

a data line group including a plurality of data lines;

a first bit line group including a plurality of bit lines;

a first column gate circuit that electrically connects the first bit line group to the data line group according to a first column selection signal;

a second bit line group including a plurality of bit lines:

a second column gate circuit that electrically connects the second bit line group to the data line group according to a second column selection signal different from the first column selection signal;

a plurality of word lines intersecting the plurality of bit lines included in the first and second bit line groups; and

a plurality of memory cells including magneto-resistive elements and adapted to be electrically connected to a plurality of bit lines included in the first and second bit line groups and selected by the plurality of word lines, the magneto-resistive elements being rectangular with short sides and long sides as seen on a plan view and the long sides intersecting the plurality of bit lines included in the first and second bit line groups as seen in a plan view.

Claim 3 (Withdrawn): A semiconductor integrated circuit device comprising:

a data line group including a plurality of data lines;

a first bit line group including a plurality of bit lines;

a first column gate circuit that electrically connects the first bit line group to the data line group according to a first column selection signal;

a second bit line group including a plurality of bit lines:

a second column gate circuit that electrically connects the second bit line group to the data line group according to a second column selection signal different from the first column selection signal;

a plurality of word lines intersecting the plurality of bit lines included in the first and second bit line groups; and

a plurality of memory cells including magneto-resistive elements and adapted to be electrically connected to a plurality of bit lines included in the first and second bit line groups and selected by the plurality of word lines, the magneto-resistive elements being parallelogramic with short sides and long sides as seen on a plan view and the long sides intersecting the plurality of bit lines included in the first and second bit line groups as seen in a plan view.

Claim 4 (Original): The device according to claim 1, wherein the pitch of arrangement of the first bit line group and the second bit line group is greater than the pitch of arrangement of the bit lines included in the first and second bit line groups.

Claim 5 (Withdrawn): The device according to claim 2, wherein the pitch of arrangement of the first bit line group and the second bit line group is greater than the pitch of arrangement of the bit lines included in the first and second bit line groups.

Claim 6 (Withdrawn): The device according to claim 3, wherein the pitch of arrangement of the first bit line group and the second bit line group is greater than the pitch of arrangement of the bit lines included in the first and second bit line groups.

Claim 7 (Original): The device according to claim 1, wherein the pitch of arrangement of the magneto-resistive elements is greater between the first and second bit line groups than in the first and second bit line groups.

Claim 8 (Withdrawn): The device according to claim 2, wherein the pitch of arrangement of the magneto-resistive elements is greater between the first and second bit line groups than in the first and second bit line groups.

Claim 9 (Withdrawn): The device according to claim 3, wherein the pitch of arrangement of the magneto-resistive elements is greater between the first and second bit line groups than in the first and second bit line groups.

Claim 10 (Original): The device according to claim 1, wherein the plurality of memory cells include transistors electrically connected to the respective magneto-resistive elements.

Claim 11 (Withdrawn): The device according to claim 2, wherein the plurality of memory cells include transistors electrically connected to the respective magneto-resistive elements.

Claim 12 (Withdrawn): The device according to claim 3, wherein the plurality of memory cells include transistors electrically connected to the respective magneto-resistive elements.

Claim 13 (Original): The device according to claim 1, wherein the plurality of memory cells include diodes electrically connected to the respective magneto-resistive elements.

Claim 14 (Withdrawn): The device according to claim 2, wherein the plurality of memory cells include diodes electrically connected to the respective magneto-resistive elements.

Claim 15 (Withdrawn): The device according to claim 3, wherein the plurality of memory cells include diodes electrically connected to the respective magneto-resistive elements.

Claim 16 (Original): The device according to claim 1, wherein the magneto-resistive elements are tunnel magneto-resistive effect elements of the double junction type having a first magnetization fixing layer, a first tunnel barrier layer, a magnetic recording layer, a second tunnel barrier layer and a second magnetization fixing layer.

Claim 17 (Withdrawn): The device according to claim 2, wherein the magneto-resistive elements are tunnel magneto-resistive effect elements of the double junction type having a first magnetization fixing layer, a first tunnel barrier layer, a magnetic recording layer, a second tunnel barrier layer and a second magnetization fixing layer.

Claim 18 (Withdrawn): The device according to claim 3, wherein the magneto-resistive elements are tunnel magneto-resistive effect elements of the double junction type having a first magnetization fixing layer, a first tunnel barrier layer, a magnetic recording layer, a second tunnel barrier layer and a second magnetization fixing layer.

Claim 19 (Original): The device according to claim 1, wherein the magneto-resistive elements are tunnel magneto-resistive effect elements having a magnetization fixing layer, a

tunnel barrier layer and a magnetic recording layer and at least the magnetization fixing layer includes a stack structure of a ferromagnetic layer and a non-magnetic layer.

Claim 20 (Withdrawn): The device according to claim 2, wherein the magneto-resistive elements are tunnel magneto-resistive effect elements having a magnetization fixing layer, a tunnel barrier layer and a magnetic recording layer and at least the magnetization fixing layer includes a stack structure of a ferromagnetic layer and a non-magnetic layer.

Claim 21 (Withdrawn): The device according to claim 3, wherein the magneto-resistive elements are tunnel magneto-resistive effect elements having a magnetization fixing layer, a tunnel barrier layer and a magnetic recording layer and at least the magnetization fixing layer includes a stack structure of a ferromagnetic layer and a non-magnetic layer.

Claim 22 (Original): The device according to claim 1, wherein the magneto-resistive elements are tunnel magneto-resistive effect elements of the double junction type having a first magnetization fixing layer, a first tunnel barrier layer, a magnetic recording layer, a second tunnel barrier layer and a second magnetization fixing layer and at least either of the first and second magnetization fixing layers and the magnetic recording layer include a stack structure of a ferromagnetic layer and a non-magnetic layer.

Claim 23 (Withdrawn): The device according to claim 2, wherein the magneto-resistive elements are tunnel magneto-resistive effect elements of the double junction type having a first magnetization fixing layer, a first tunnel barrier layer, a magnetic recording layer, a second tunnel barrier layer and a second magnetization fixing layer and at least either

of the first and second magnetization fixing layers and the magnetic recording layer include a stack structure of a ferromagnetic layer and a non-magnetic layer.

Claim 24 (Withdrawn): The device according to claim 3, wherein the magneto-resistive elements are tunnel magneto-resistive effect elements of the double junction type having a first magnetization fixing layer, a first tunnel barrier layer, a magnetic recording layer, a second tunnel barrier layer and a second magnetization fixing layer and at least either of the first and second magnetization fixing layers and the magnetic recording layer include a stack structure of a ferromagnetic layer and a non-magnetic layer.